Computer Architecture

Short Notes based on ***Exit Exam***

Zemzem labs

1. Introduction to Computer Architecture

Computer Architecture vs Organization

- **Architecture:** What the system does (instruction set, addressing modes)
- **Organization:** How it is implemented (hardware, signals, control)

Basic Components

- CPU (ALU + Control Unit)
- Memory
- I/O devices
- System bus

2. CPU Organization

CPU Components

1. **ALU (Arithmetic Logic Unit)**
2. **Control Unit (CU)**
3. **Registers**

Types of Registers

- Program Counter (PC)
- Instruction Register (IR)
- Memory Data Register (MDR)
- Accumulator
- General Purpose Registers
- Status Register (Flags)

Instruction Cycle

1. Fetch
2. Decode
3. Execute
4. Memory access (optional)
5. Write-back

3. Instruction Set Architecture (ISA)

Types of Instruction Sets

- **RISC (Reduced)**
  - Simple, fixed-length instructions
  - Load/Store architecture
  - Examples: ARM, MIPS
- **CISC (Complex)**
  - Many complex instructions
  - Variable-length instructions
  - Example: x86

Addressing Modes

- Immediate
- Direct
- Indirect
- Register
- Register Indirect
- Indexed
- Base-register
- Relative addressing

4. Memory Organization

Memory Hierarchy

1. Registers
2. Cache
3. Main memory (RAM)
4. Secondary storage

Faster = smaller = expensive.

Cache Memory

- Stores frequently used data
- Reduces average access time

Cache Mapping Techniques

- Direct mapping
- Fully associative
- Set associative

Cache Terms

- Hit / Miss
- Hit ratio
- Miss penalty

Memory Types

- SRAM → used in cache
- DRAM → used in main memory
- ROM → non-volatile

5. Pipelining

Improves CPU throughput by overlapping instruction execution.

Stages (typical 5-stage pipeline):

1. IF – Instruction Fetch
2. ID – Instruction Decode
3. EX – Execute
4. MEM – Memory Access
5. WB – Write Back

Pipeline Hazards

- **Structural hazards** – resource conflicts
- **Data hazards** – read-after-write (RAW)
- **Control hazards** – branch hazards

Solutions

- Forwarding
- Stalling
- Branch prediction

6. Input/Output Organization

I/O Techniques

- Programmed I/O
- Interrupt-driven I/O
- DMA (Direct Memory Access) → fastest I/O

Types of Interrupts

- Hardware
- Software
- Maskable
- Non-maskable

I/O Mapping

- Memory-mapped I/O
- Isolated I/O

7. Arithmetic & Logic

Number Systems

- Binary
- Octal
- Decimal
- Hexadecimal

Signed Number Representations

- Sign magnitude
- 1's complement
- 2's complement (most common)

Floating-Point Numbers

- IEEE 754 standard
- Contains:
    - Sign bit
    - Exponent
    - Mantissa (fraction)

8. ALU Design

Operations

- Addition, subtraction
- AND, OR, XOR
- Shift operations (logical, arithmetic)

Carry Lookahead Adder

Speeds up addition using parallel carry computation.

9. Control Unit

Hardwired Control

- Fast
- Difficult to modify
- Circuit-based

Micro-programmed Control

- Slower
- Flexible
- Control stored in control memory (microcode)

10. Bus Structure

System Bus Types

- Data bus
- Address bus
- Control bus

Bus Arbitration

- Daisy chaining
- Centralized arbitration
- Distributed arbitration

11. Multiprocessors & Parallelism

Types of Parallelism

- Instruction-level
- Data-level
- Thread-level

Flynn's Taxonomy

- SISD — single instruction, single data
- SIMD — single instruction, multiple data
- MISD — multiple instruction, single data
- MIMD — multiple instruction, multiple data

Shared Memory vs Distributed Memory

- Shared → multiple CPUs access same RAM
- Distributed → each CPU has its own memory

12. RISC vs CISC (Detailed)

RISC Characteristics

- Simple instruction set
- One instruction per cycle
- Fixed-length instructions
- Emphasizes pipelines
- Example: ARM

CISC Characteristics

- Complex instructions
- Variable-length
- Less registers
- Example: Intel x86

13. Virtual Memory

Purpose

Allows programs to use more memory than physically available.

Techniques

- Paging
- Segmentation

Page Fault

Occurs when required page is not in memory.

Replacement Algorithms

- FIFO
- LRU
- Optimal

🌟 Ultra-Condensed Exam Summary

- Architecture defines instruction set; organization defines implementation
- RISC = simple + fast pipelining; CISC = complex
- Cache = fast memory with direct/associative/set-associative mapping
- Pipeline hazards = data, structural, control
- DMA = fastest I/O method
- IEEE 754 for floating point
- Flynn's taxonomy: SISD/SIMD/MISD/MIMD
- Virtual memory uses paging → page faults → replacement algorithms